CLAIMS

1. An apparatus for current leakage correction coupled to a leaky capacitor, comprising:

a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

a plurality of current mirrors, wherein the plurality of current mirrors further comprise:

at least one current mirror is at least configured to be coupled to the leaky capacitor; and

at least one current mirror is at least configured to be coupled to the scaled capacitor that is at least configured to provide a potential difference across the scaled capacitor that is substantially equal to a potential difference across the leaky capacitor.

2. The apparatus of Claim 1, wherein the plurality of current mirror further comprises a plurality of transistors.

3. The apparatus of Claim 1, wherein the plurality of current mirrors further comprises a plurality of Field Effect Transistors (FET).

4. The apparatus of Claim 3, wherein at least one FET of the plurality of FETs is a Positive-Channel FET (PFET),

wherein the PFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

5. The apparatus of Claim 4, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

6. The apparatus of Claim 3, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

7. The apparatus of Claim 1, wherein the plurality of current mirrors further comprise a plurality of bipolar transistors.

8. The apparatus of Claim 1, wherein the plurality of current mirrors further comprise a plurality of Metal-Oxide Semiconductor FETs (MOSFETs).

9. The apparatus of Claim 8, wherein at least one MOSFET of the plurality of MOSFETs is a Positive-type MOSFET (P-type MOSFET), wherein the P-type MOSFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

10. The apparatus of Claim 9, wherein at least one FET of the plurality of FETs is a Negative-type MOSFET (N-type MOSFET).

11. The apparatus of Claim 8, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

12. A method for current leakage correction for a leaky capacitor, comprising:

measuring voltage across the leaky capacitor;

providing the measured voltage to a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

providing a sustaining charge to the leaky capacitor.

13. The method of Claim 12, wherein the step of providing the measured voltage to a scaled capacitor further comprises utilizing a plurality of current mirrors with an adjusted width and length to provide the measured voltage to the scaled capacitor.

14. A computer program product for current leakage correction for a leaky capacitor in a computer system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for measuring voltage across the leaky capacitor;

computer code for providing the measured voltage to a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

computer code for providing a sustaining charge to the leaky capacitor.

15. The computer program product of Claim 14, wherein the computer code for providing the measured voltage to a scaled capacitor further comprises computer code for utilizing a plurality of current mirrors with an adjusted width and length to provide the measured voltage to the scaled capacitor.

16. A circuit for current leakage correction coupled to a leaky capacitor, comprising:

a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

a plurality of current mirrors, wherein the plurality of current mirrors further comprise:

at least one current mirror is at least configured to be coupled to the leaky capacitor; and

at least one current mirror is at least configured to be coupled to the scaled capacitor that is at least configured to provide a potential difference across the scaled capacitor that is substantially equal to a potential difference across the leaky capacitor.

17. The circuit of Claim 16, wherein the plurality of current mirror further comprises a plurality of transistors.

18. The circuit of Claim 16, wherein the plurality of current mirrors further comprises a plurality of Field Effect Transistors (FET).

19. The circuit of Claim 18, wherein at least one FET of the plurality of FETs is a Positive-Channel FET (PFET), wherein the PFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

20. The circuit of Claim 19, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

21. The circuit of Claim 18, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

22. The circuit of Claim 16, wherein the plurality of current mirrors further comprise a plurality of bipolar transistors.

23. The circuit of Claim 16, wherein the plurality of current mirrors further comprise a plurality of Metal-Oxide Semiconductor FETs (MOSFETs).

24. The circuit of Claim 23, wherein at least one MOSFET of the plurality of MOSFETs is a Positive-type MOSFET (P-type MOSFET), wherein the P-type MOSFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

25. The circuit of Claim 24, wherein at least one FET of the plurality of FETs is a Negative-type MOSFET (N-type MOSFET).

26. The circuit of Claim 23, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).